

MY2 (Milo2-H)

BLOCK DIAGRAM

Intel Huron River Sandy bridge UMA

01

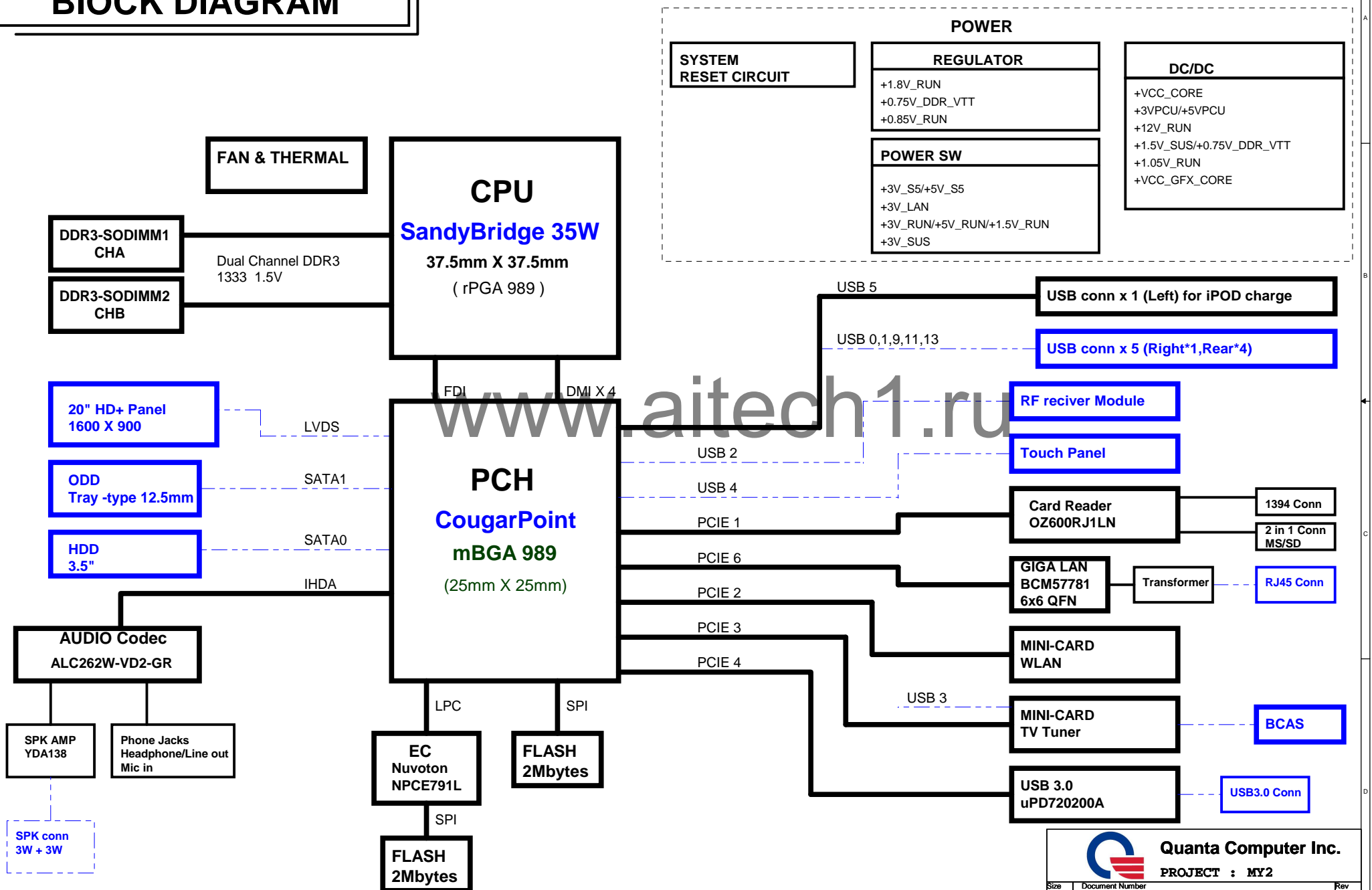


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MY2 Milo2 Power Rails

MY2(Milo2) Power On Sequence

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Power	Voltage	S0	S3	S4	S5	Ctl Signal
+5VPCU	5V	V	V	V	V	6237LDO5
+3VPCU	3.3V	V	V	V	V	6237LDO5
+3V_LAN	3.3V	V	NOTE 1	NOTE 1	NOTE 1	LAN_ON_D
+5V_S5	5V	V	V	NOTE 2	NOTE 2	RVCCD
+3V_S5	3.3V	V	V	NOTE 2	NOTE 2	RVCCD
+1.5V_SUS	1.5V	V	V			SUSON
+DDR_VTTREF	0.75V	V	V			+1.5V_CPUVDDQ_PG
+3V_SUS	3.3V	V	V			SUSD
+0.75V_DDR_VTT	0.75V	V				+1.5V_CPUVDDQ_PG
+12V_RUN	12V	V				RUN_ON
+5V_RUN	5V	V				MAIND
+3V_RUN	3.3V	V				MAIND
+1.8V_RUN	1.8V	V				+3V_RUN
+1.5V_RUN	1.5V	V				MAIND
+1.05V_RUN	1.05V	V				RUN_ON
+0.85V_RUN	0.85V	V				1.05V_VTT_PWRGD
+VCC_GFX_CORE	By VID	V				ALL_SYS_PWRGD
+VCC_CORE	By VID	V				ALL_SYS_PWRGD

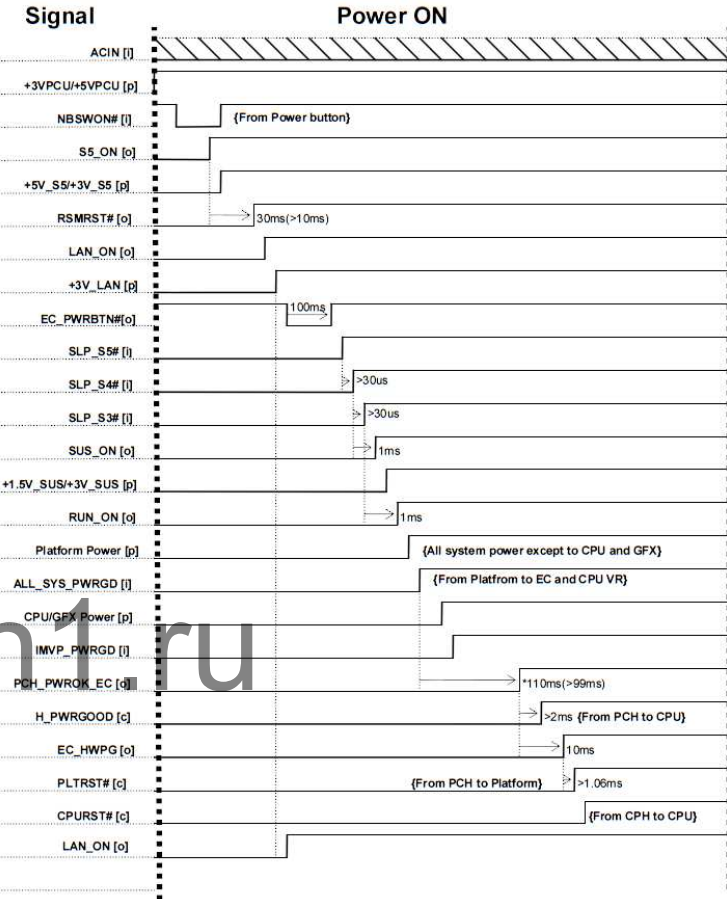
NOTE 1: ON AT WOL FUNCTION ENABLE

NOTE 2: ON FOR WAKE UP FUNCTION DURING S4/S5

PCB STACK UP

6L

LAYER 1 : TOP
LAYER 2 : VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : BOT

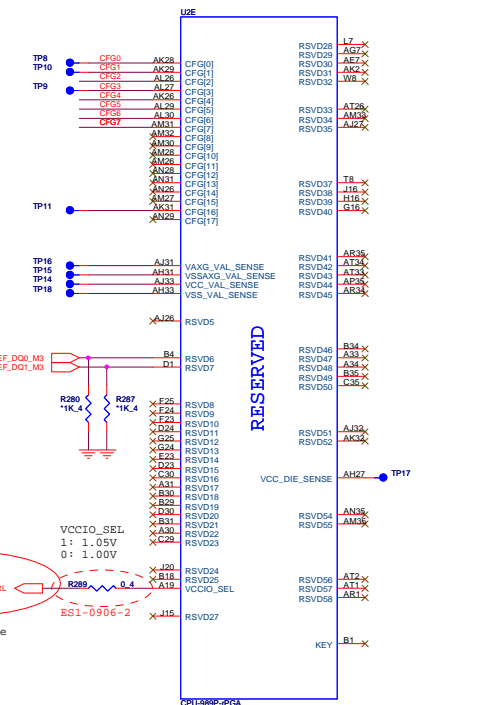
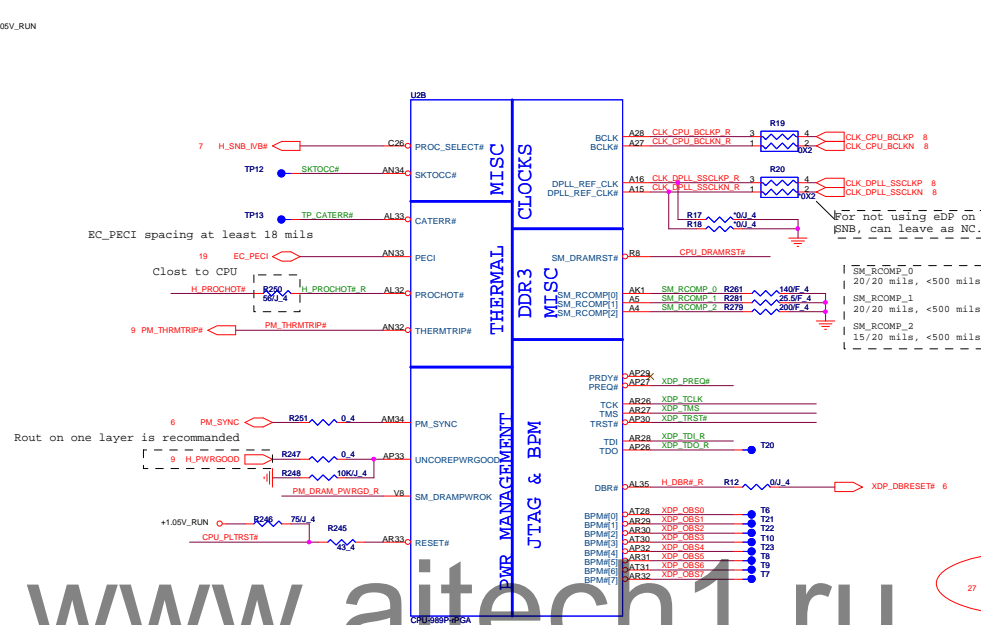


*Note: PCH_PWROK_EC should wait for both ALL_SYS_PWRGD and IMVP_PWRGD ready.

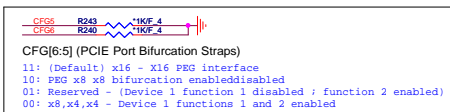
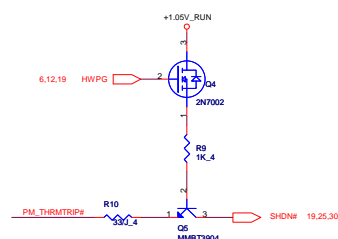
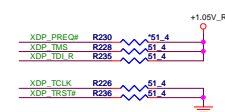
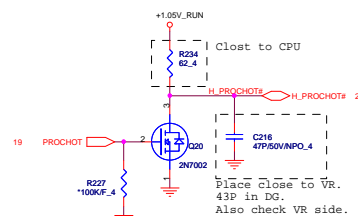
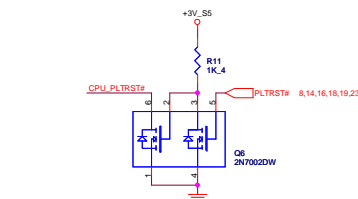
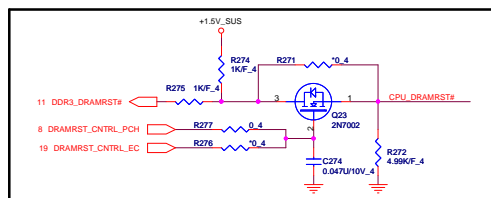
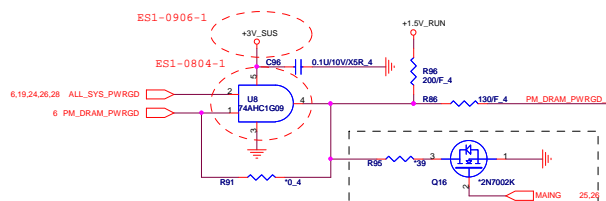
Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

Sandy Bridge Processor (RSVD, CFG)



Check:
Follow Intel demo schematic and power sequence spec.
Is it possible that PM_DRAM_PWRD connects to PM_DRAM_PWRGD_R?

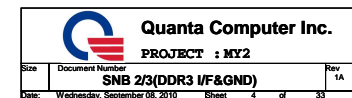


The CFG signals have a default value of '1' if not terminated on the board.

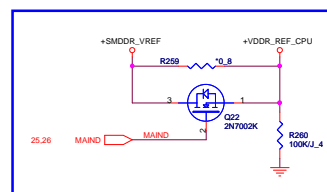
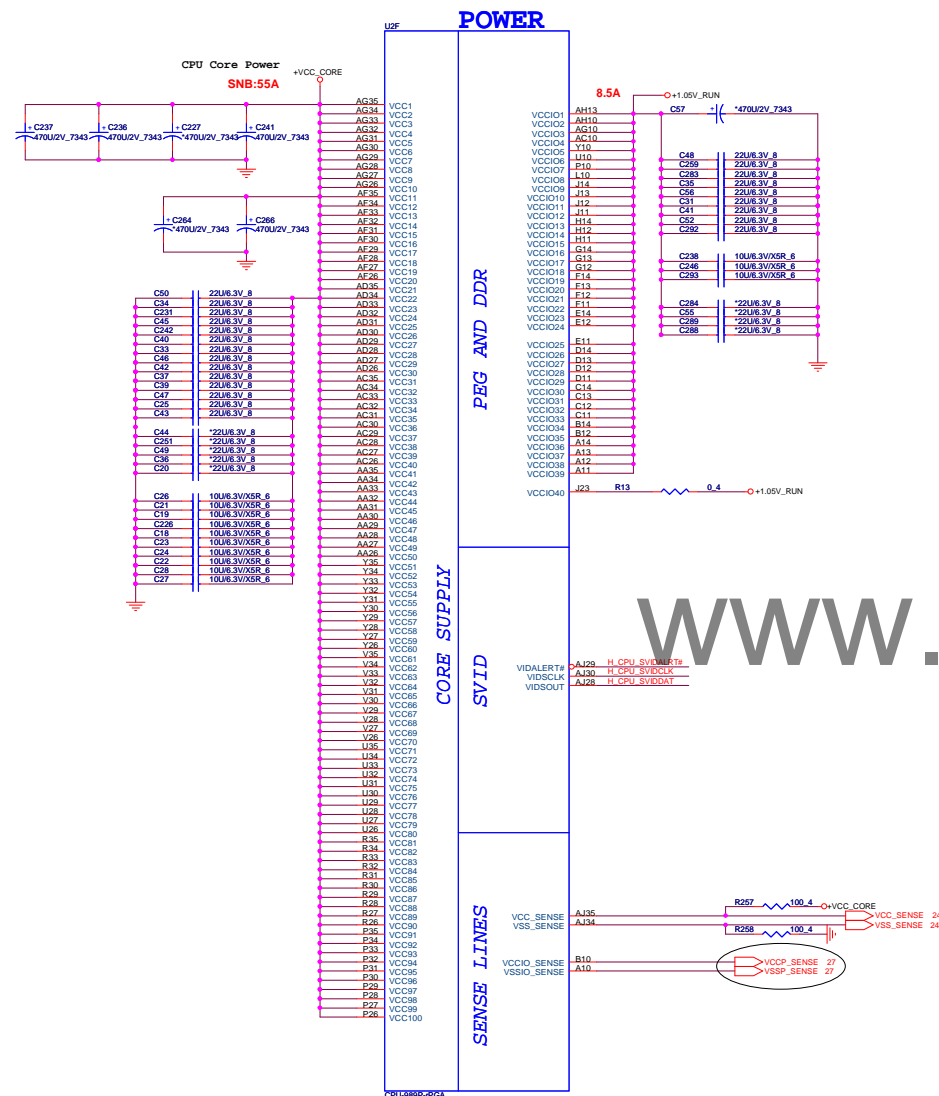
Processor Strapping

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xRESETB of assertion	PEG wait for BIOS training

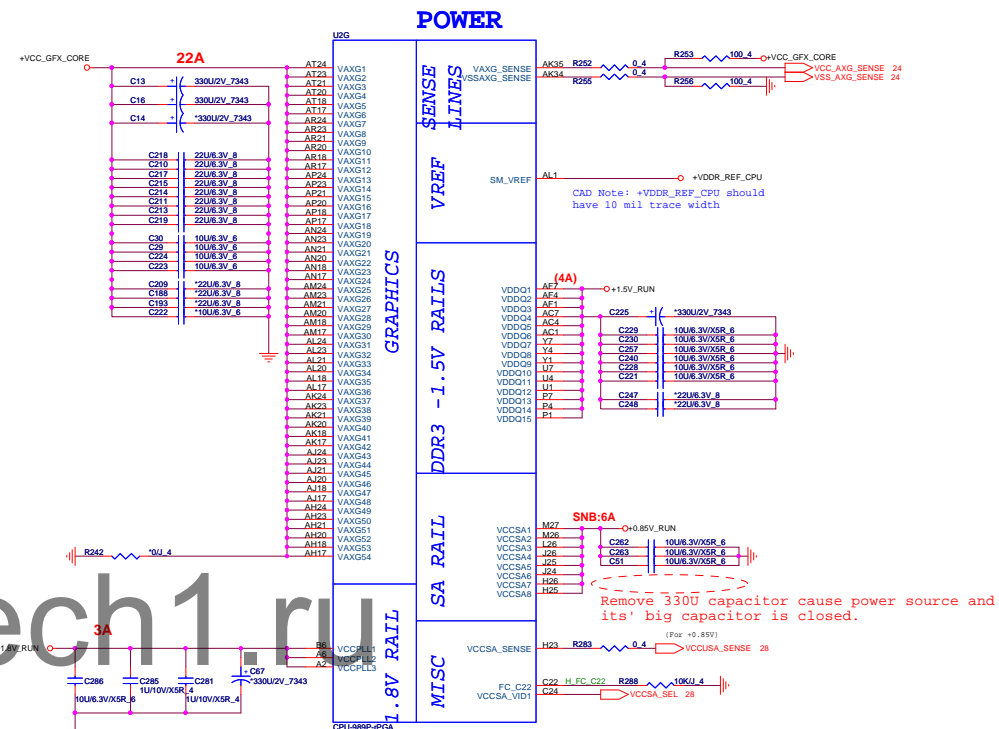
Sandy Bridge Processor (GND)



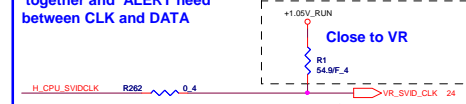
Sandy Bridge Processor (POWER)



Sandy Bridge Processor (GRAPHIC POWER)



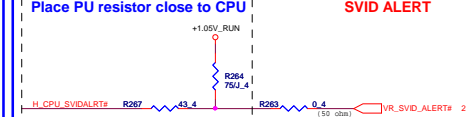
Layout note: need routing together and ALERT need between CLK and DATA



- Place PU resistor close to CPU

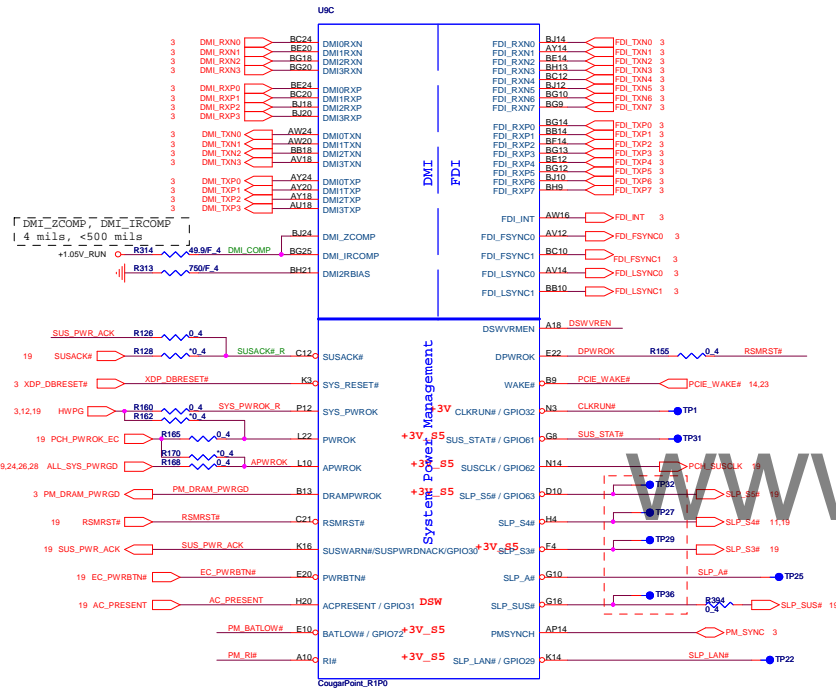


- Place PU resistor close to CPU

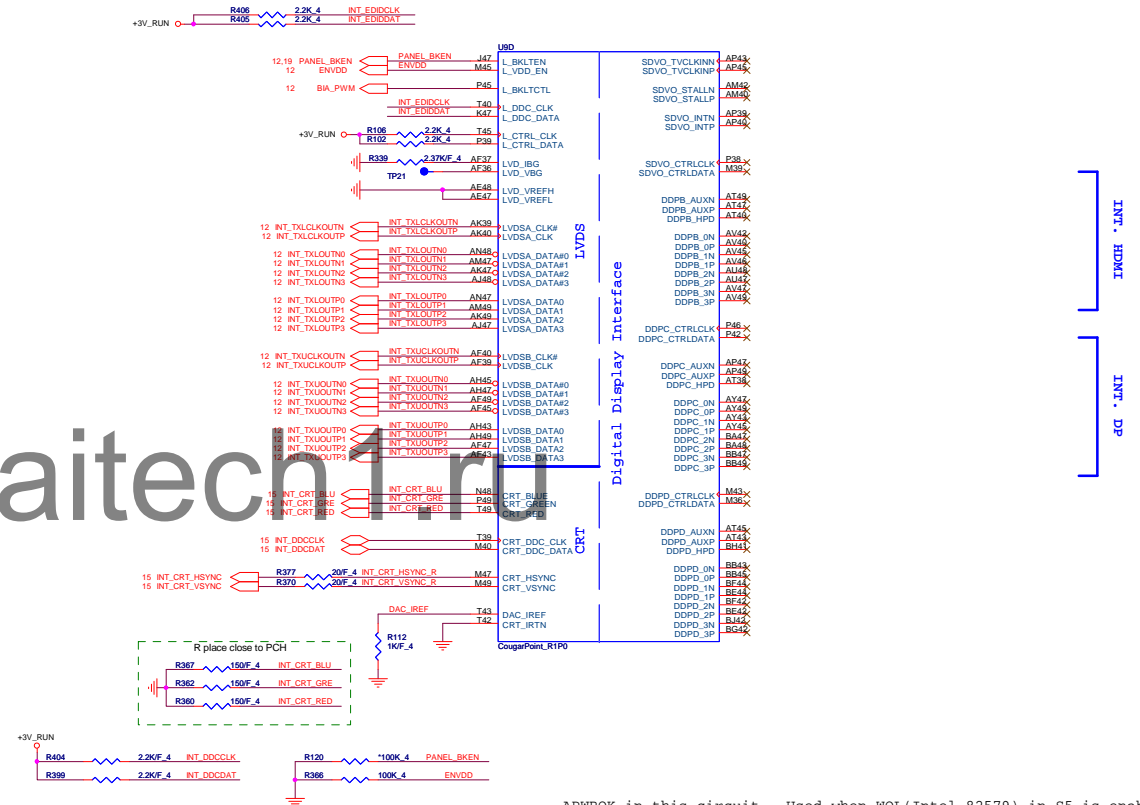


PCH 1/5 (DMI/FDI/VIDEO)

Cougar Point (DMI,FDI,PM)

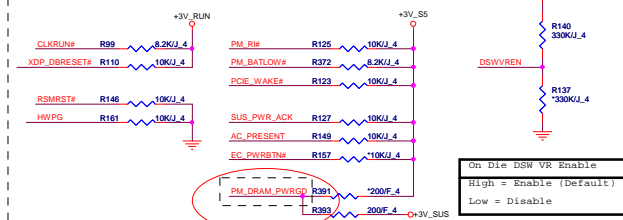


Cougar Point (LVDS,DDI)



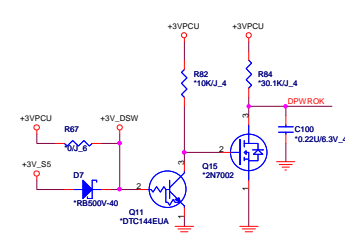
APWROK in this circuit---Used when WOL(Intel 82579) in S5 is enable.
For Non-INTEL LAN--Reserved

PCH Pull-high/low(CLG)

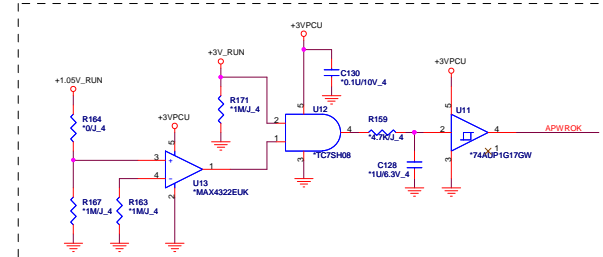


This segment should less
than 500 mils.

```
(RSMRST# connect to DPWROK --
it will make a period of 10 ms)
```



If +3V_DSW connected to +3V_S5, it will never get DEEP S4/S5 state in this schematic??

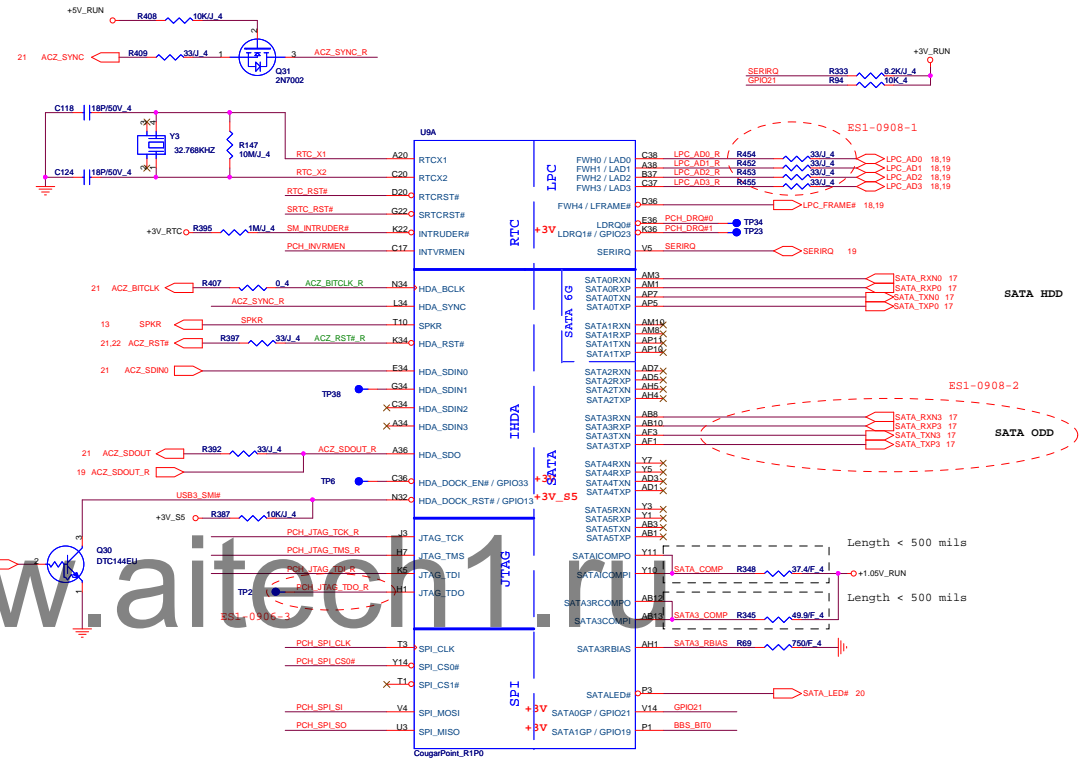
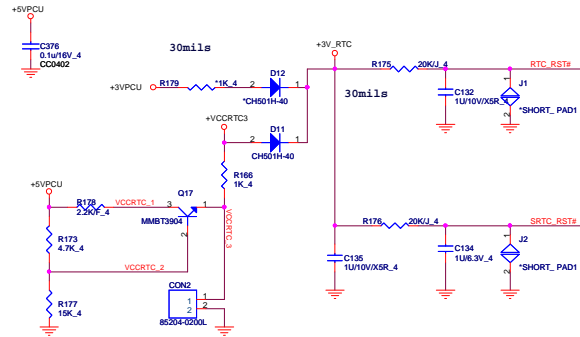


PCH 2/5(SATA/RTC/HDA/LPC)

07

Cougar Point (HDA,JTAG,SATA)

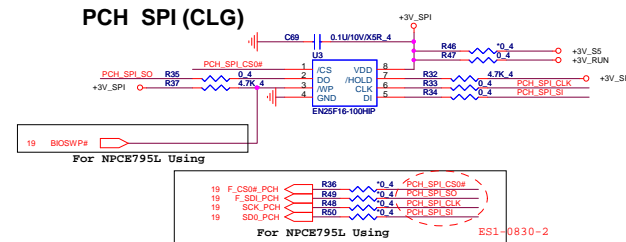
RTC Circuitry (RTC) (Rechargeable BATT)



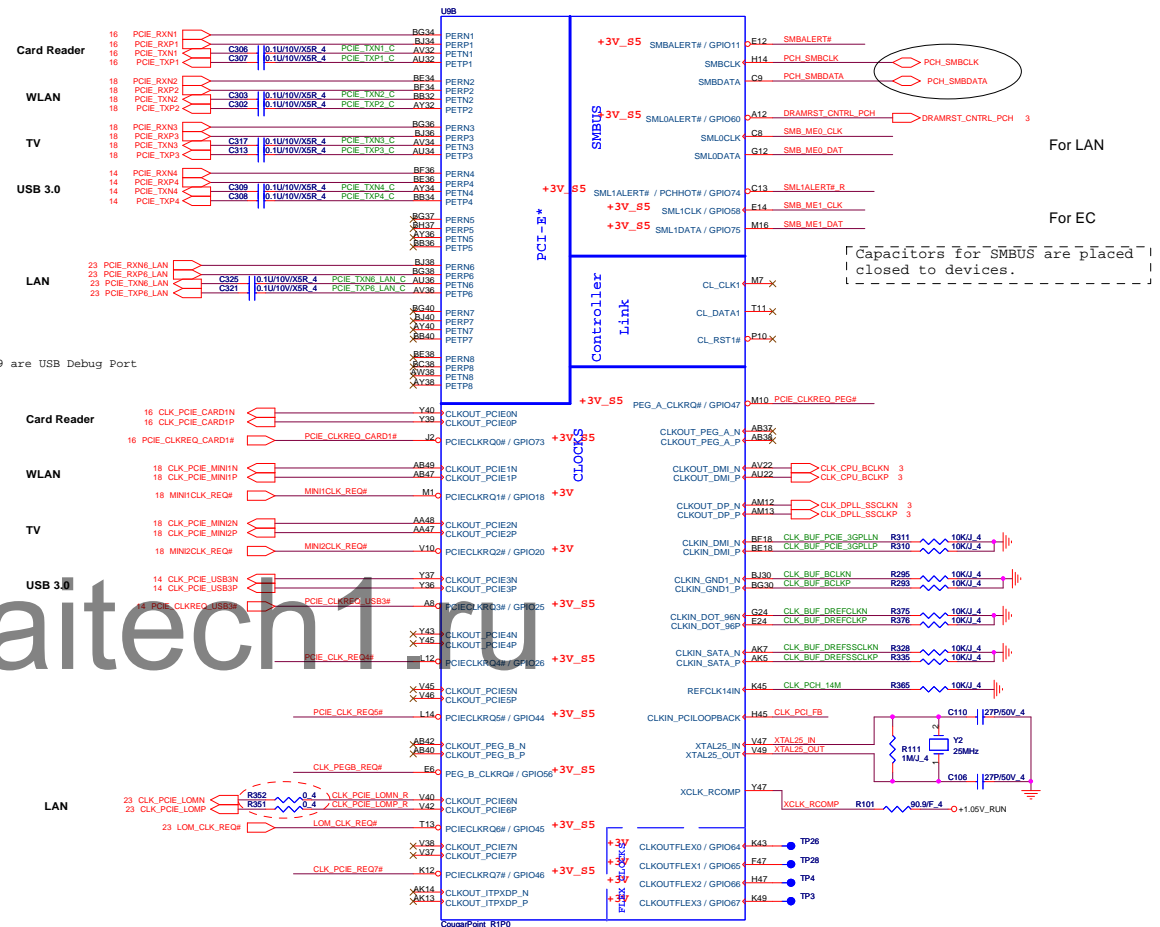
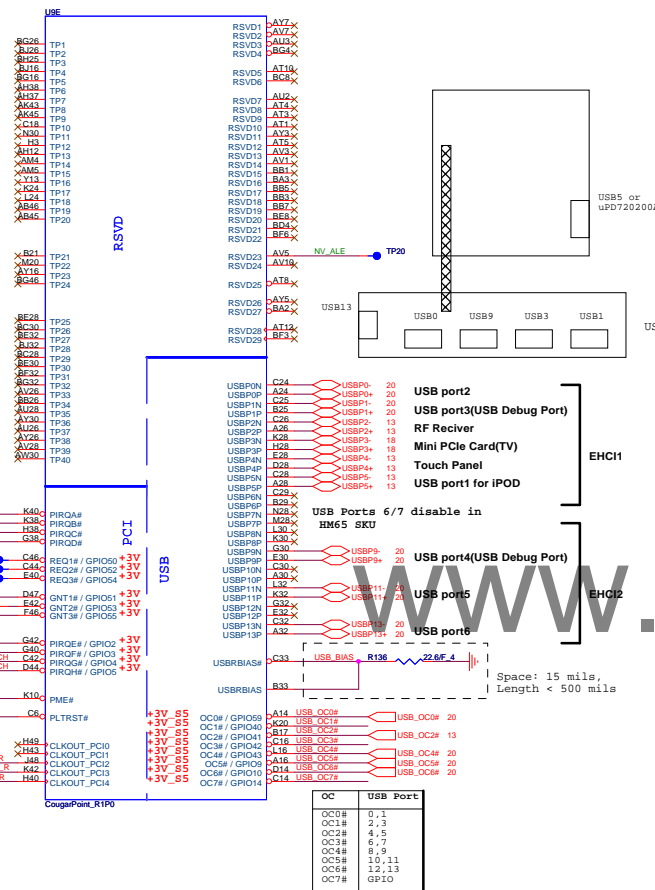
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V_RUN - R103 - 1K_4 - SPCR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R121 - 1K_4 - PCL_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC - R139 - 330K_4 - PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]	
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3V_RUN - R389 - 1K_4 - ACZ_SDOOUT_R
DF_TV5	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R42 - 2.2K_4 - O+1.8V_RUN R41 - 4.7K_4 - DF_TV5 9 H_SNB_IVB# 3
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R359 - 1K_4 - PLL_OVR_EN 9
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_SS - R402 - 1K_4 - ACZ_SYNC_R

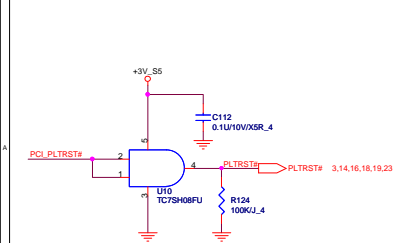
PCH SPI (CLG)



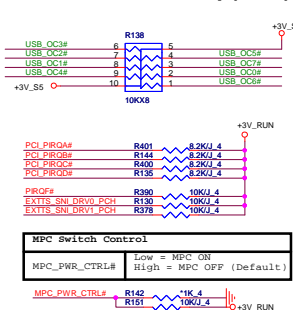
Cougar Point (PCI-E,SMBUS,CLK)



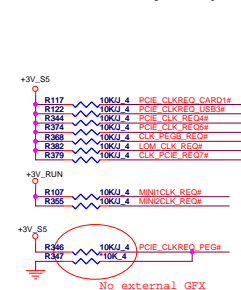
PLTRST#(CLG)



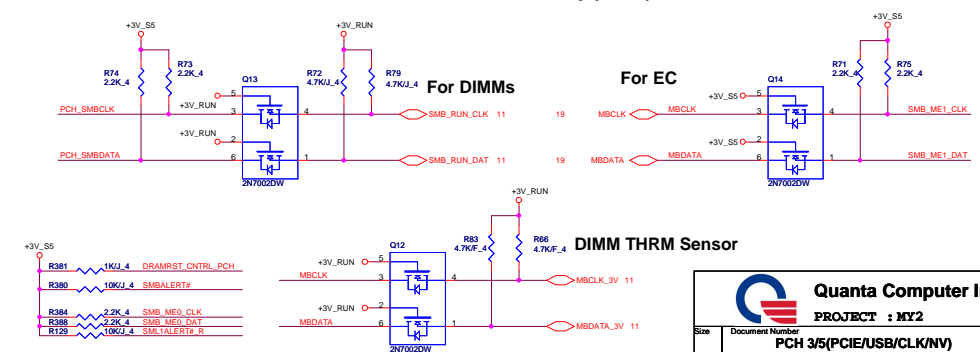
PCI/USBOC# Pull-up(CLG)



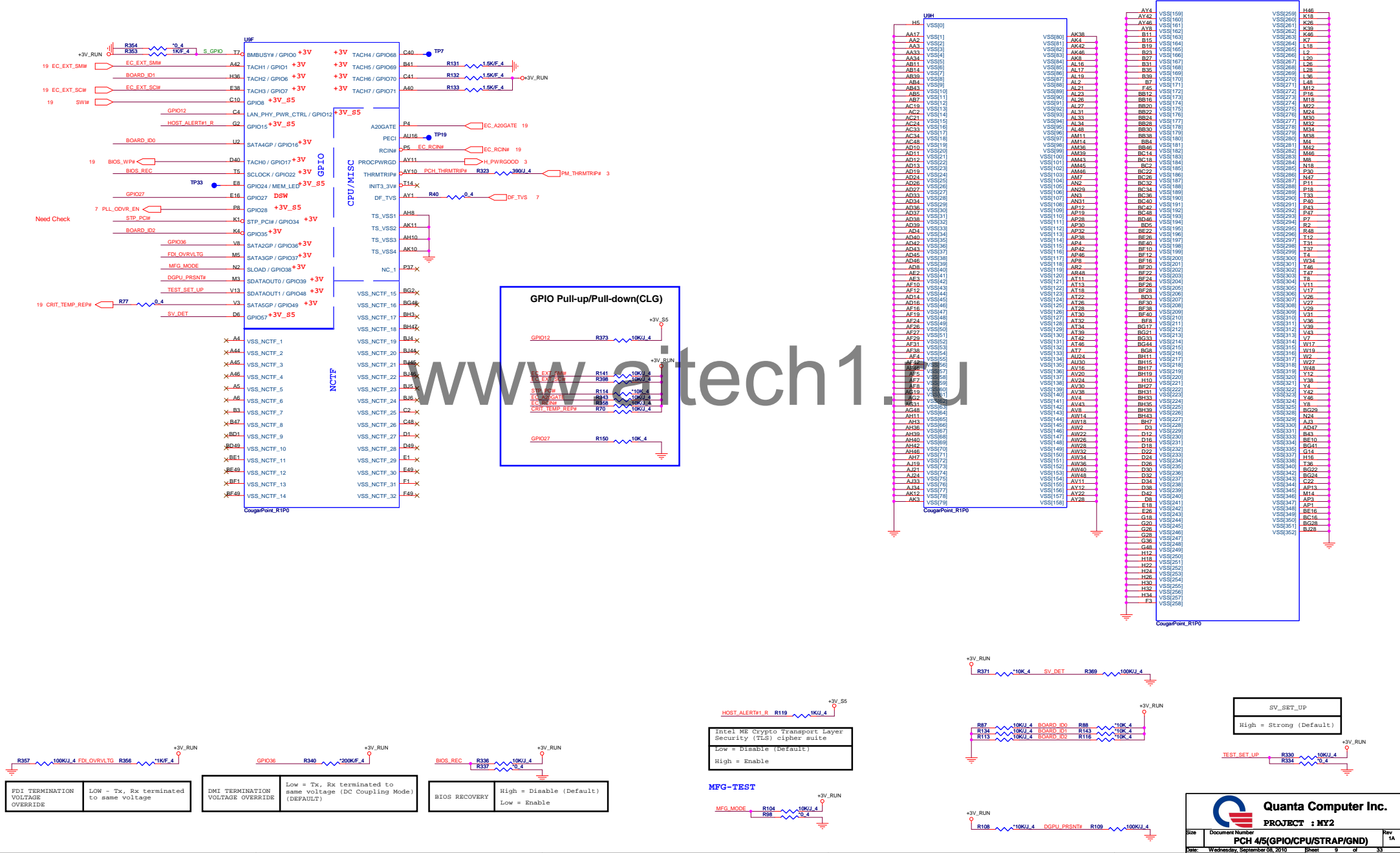
CLK_REQ/Strap Pin(CLG)



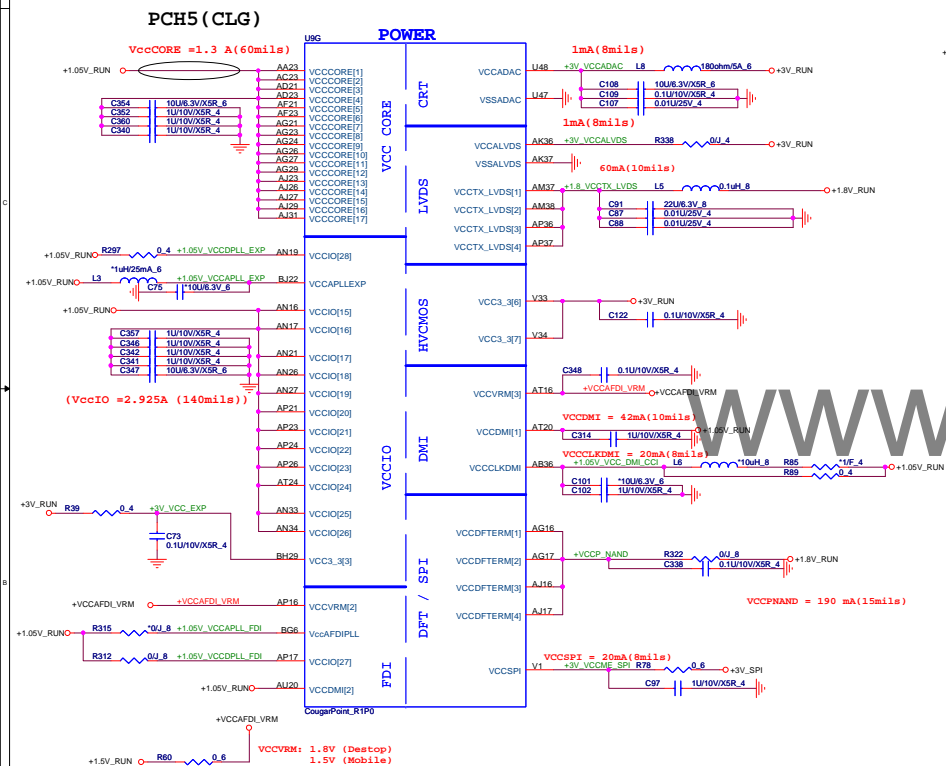
SMBus/Pull-up(CLG)



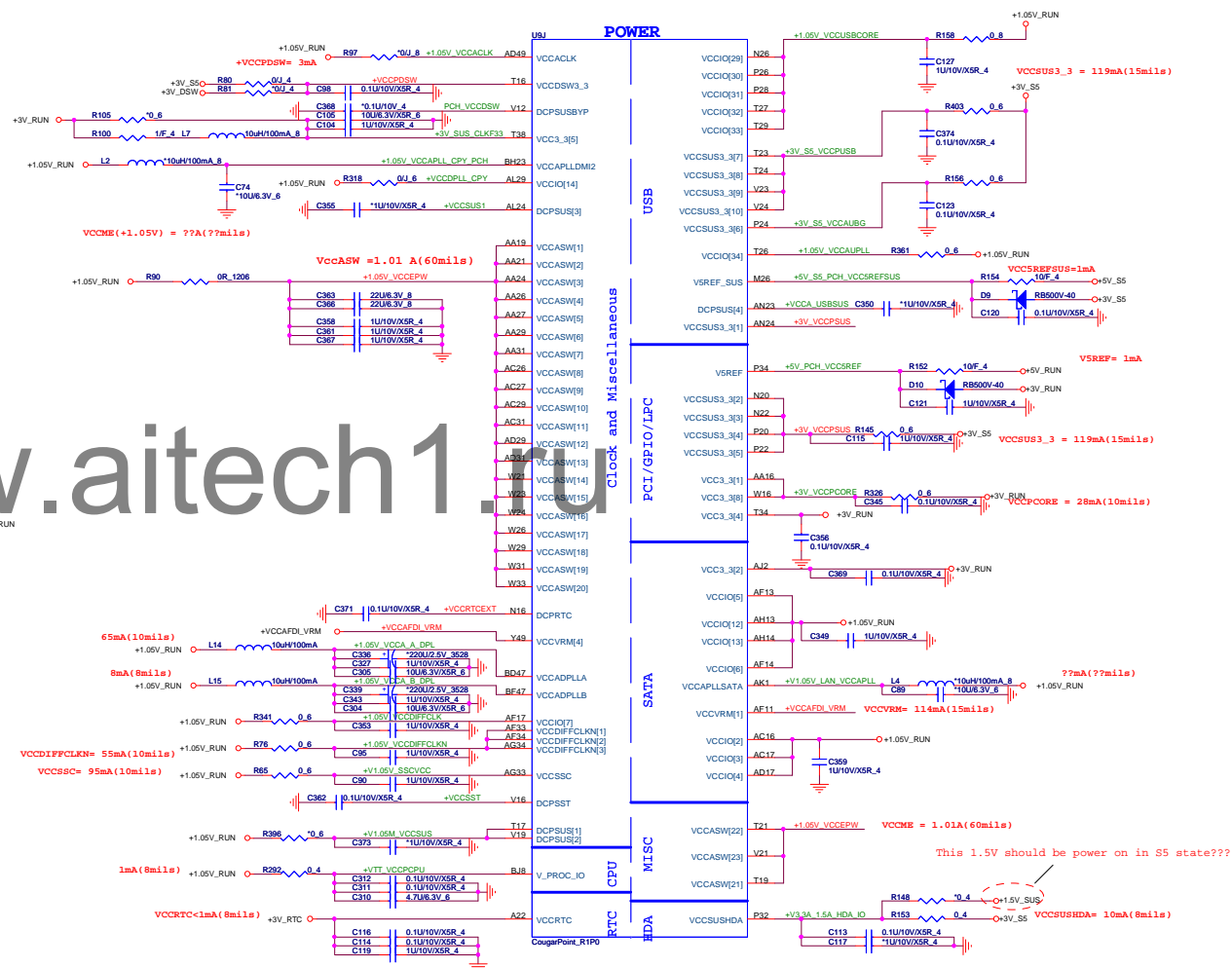
Cougar Point (GND)



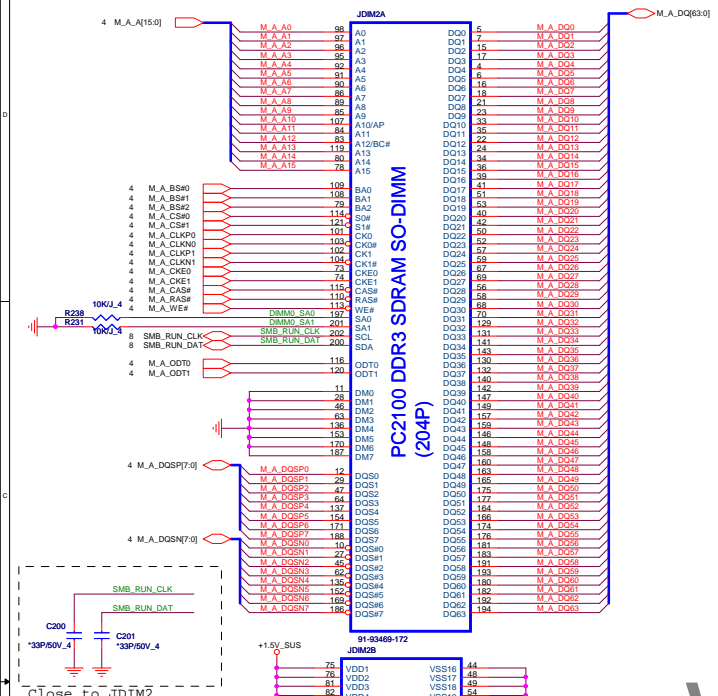
Cougar Point (POWER)



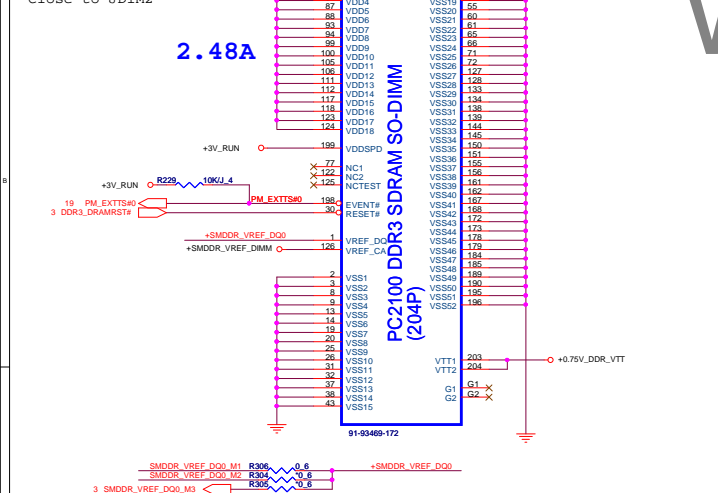
Cougar Point (POWER)



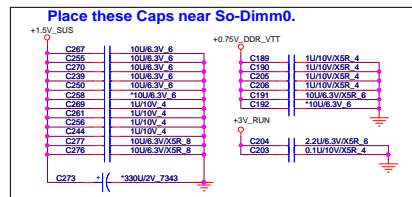
DDR3 DIMM-0-STD(9.2H)



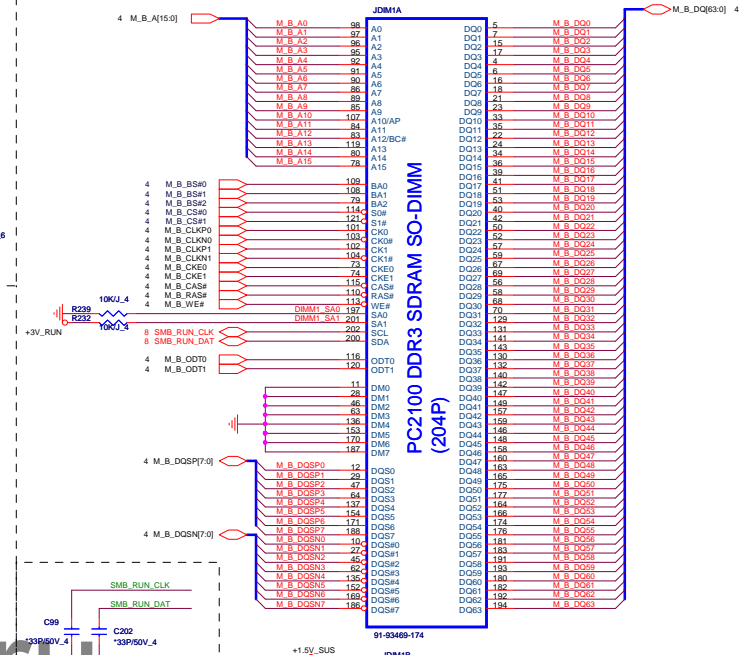
2.48A



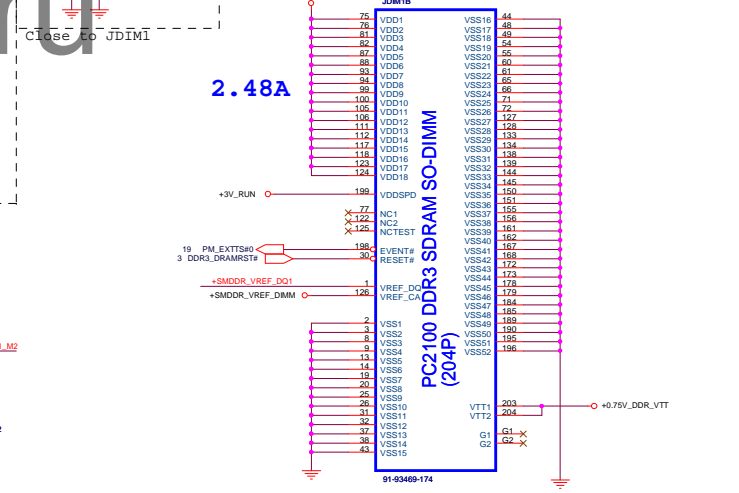
Place these Caps near So-Dimm0



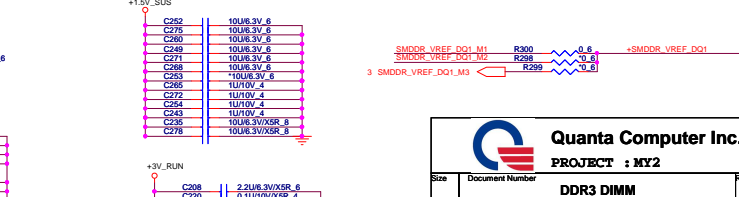
DDR3 DIMM-1-STD(5.2H)



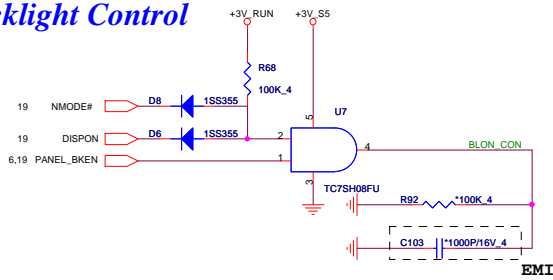
2.48A



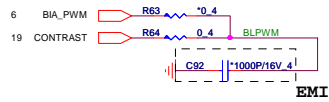
Place these Caps near So-Dimm1



Backlight Control

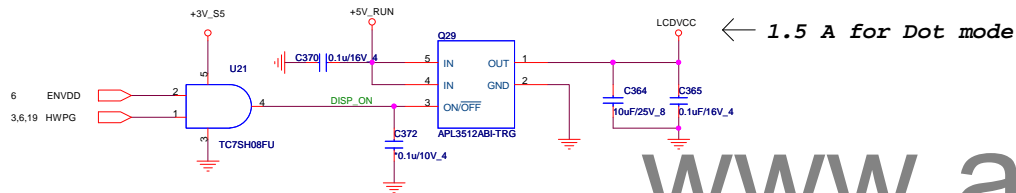


LCD backlight level Control

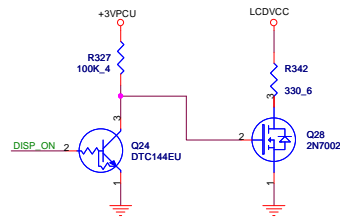


LCD POWER SWITCH(LVDS)

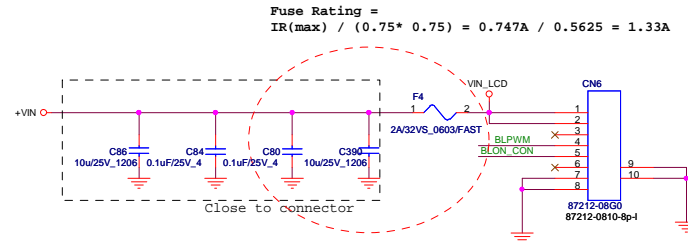
$$\text{Fuse Rating} = \frac{\text{IR(max)}}{(0.75 * 0.75)} = \frac{1.5\text{A}}{0.5625} = 2.66\text{A}$$



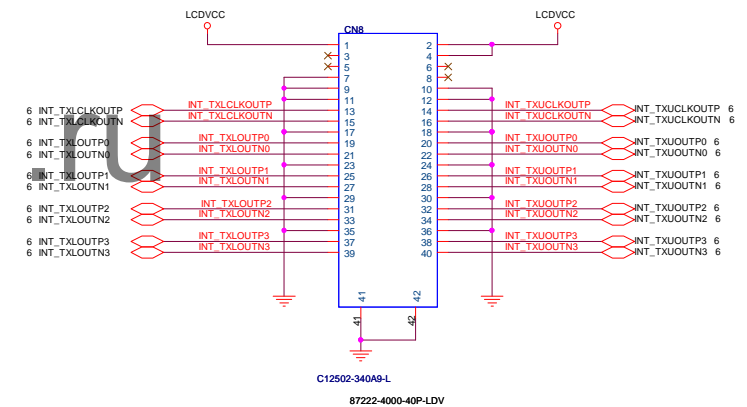
Discharge for LCD Power



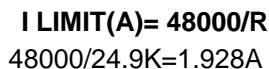
Converter Connector



LVDS Connector 20" HD+ LED backlight Panel



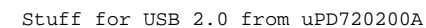
www.aitech1.ru



CTL_1	CTL_2	CTL_3	MODE
0	0	0	Turn off pwer switch & discharge VBUS
0	0	1	Auto Detect (DCP) (S3/S5)
0	1	0	SDP(S3/S5)
0	1	1	Auto Detect (DCP) (S3/S5)
1	1	0	SDP (S0)
1	1	1	CDP (S0)

Stuff for USB 2.0 from uPD720200A

CHRG OFF				CHRG ON			
S0:	CDP	1	1	1	CDP	1	1
S3:	CDP	1	1	1	DCP	0	1
S4/S5:	DCP	0	1	1	DCP	0	1

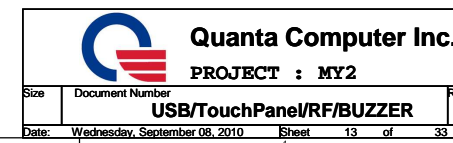


Stuff for USB 2.0 from PCH

100 miles

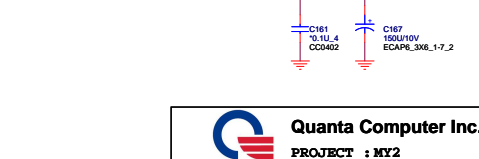
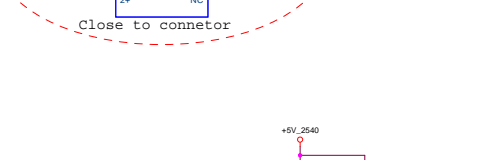
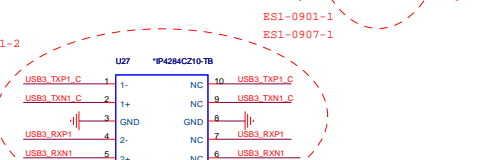
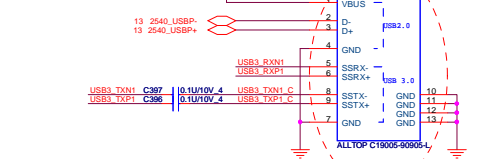
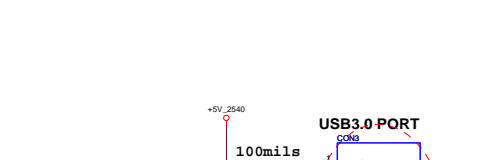
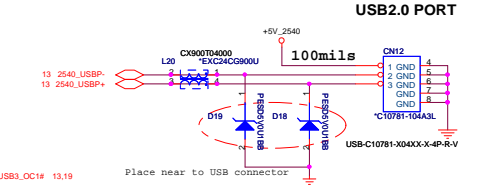
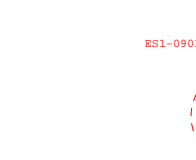
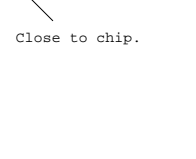
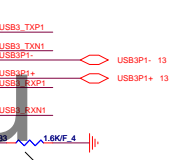
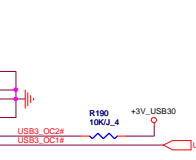
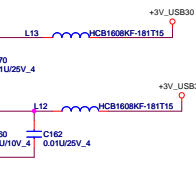
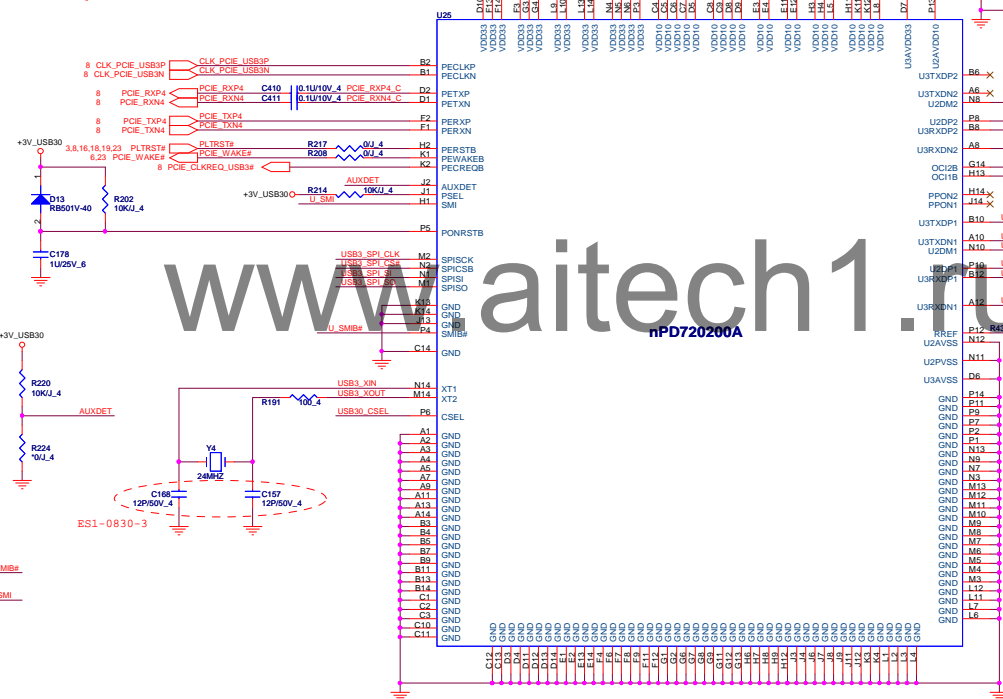
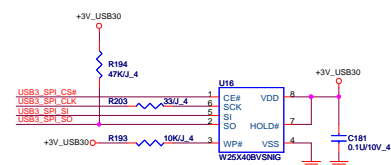
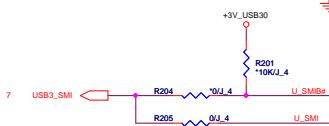
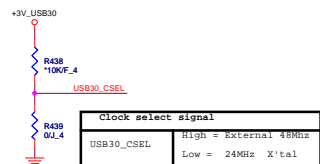
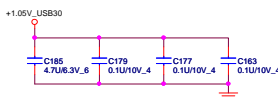
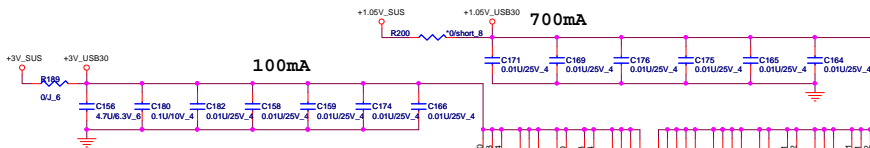
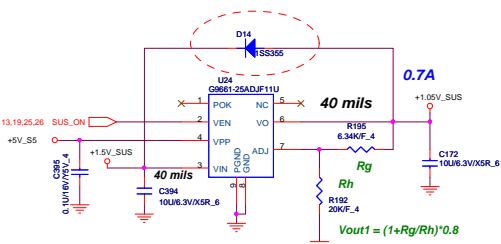
Touch Panel CONN(Reserved)

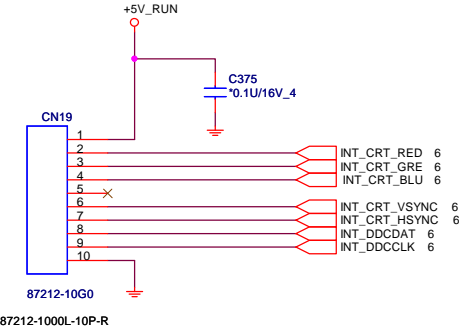
Buzzer



USB3.0

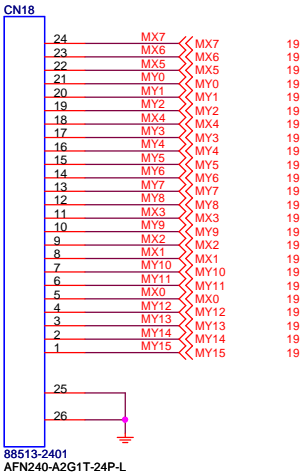
+1.05V_SUS





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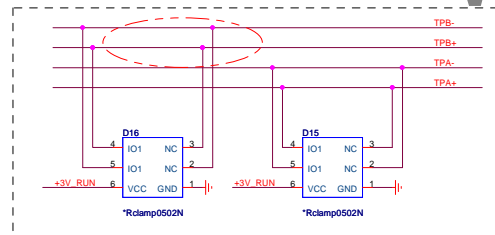
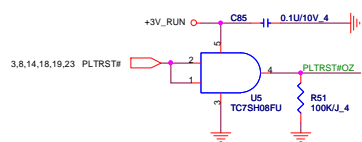
Keyboard(KBC)
Reserve ND3 Keyboard for Debug **KEYBOARD**



NOTE2:
THESE PCI EXPRESS SIGNALS ARE HIGH SPEED DIFFERENTIAL PAIRS AND MUST BE KEPT EQUAL LENGTH WITH A DIFFERENTIAL IMPEDANCE (Z0) OF 100 OHMS. EACH LANE OF THE DIFFERENTIAL SIGNAL PAIR MUST BE AC-COUPLED.

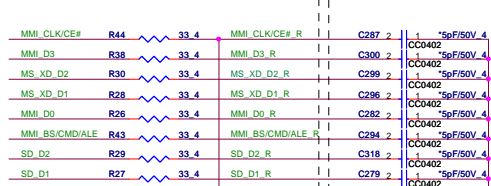
NOTE3:
THIS 100MHZ REFERENCE CLOCK IS HIGH SPEED DIFFERENTIAL PAIR AND MUST BE KEPT EQUAL LENGTH WITH A DIFFERENTIAL IMPEDANCE (Z0) OF 100 OHMS. A DC CONNECTION FROM THE CLOCK DRIVER OUTPUT TO THE OZ600RJ1LN INPUT IS REQUIRED.

NOTE 5:
THESE 1394 SIGNALS ARE HIGH SPEED DIFFERENTIAL PAIRS AND MUST BE KEPT EQUAL LENGTH WITH A DIFFERENTIAL IMPEDANCE (Z0) OF 110 OHMS.



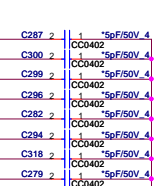
Close to connector

Close to OZ600RJ1LN-B

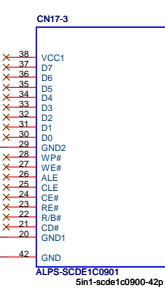


ES1-0901-3

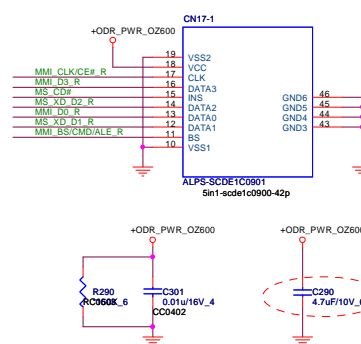
Close to socket



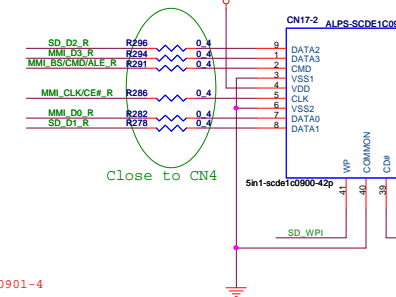
XD Socket(Non)



MemoryStick Socket

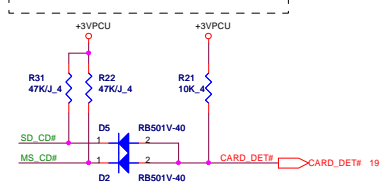


SD Socket

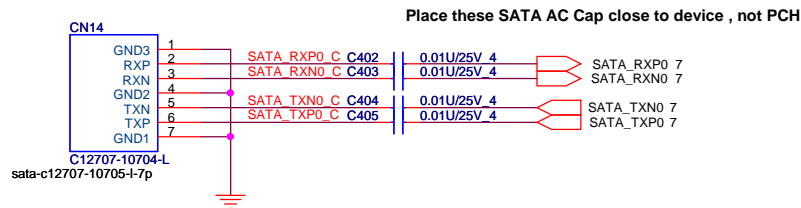


Close to CN4

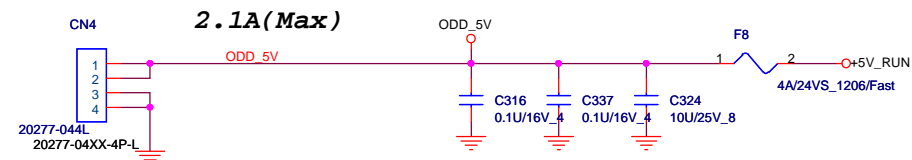
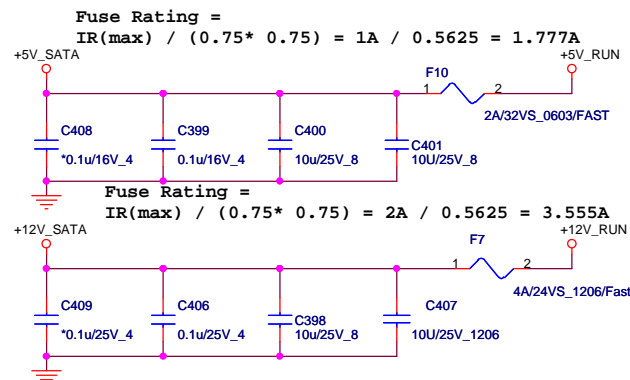
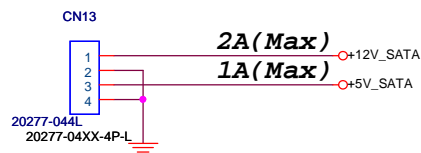
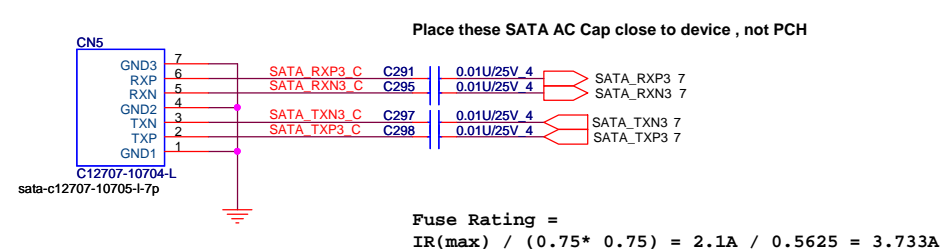
CARD_DET# at System Off
LO: Card Insert
HI: No Card



3.5" SATA HDD



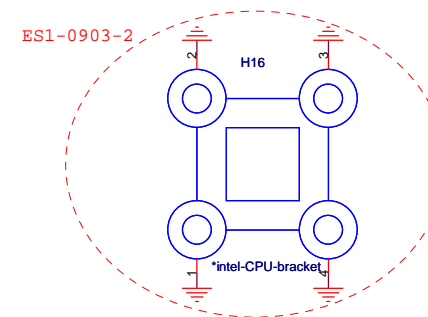
SATA ODD



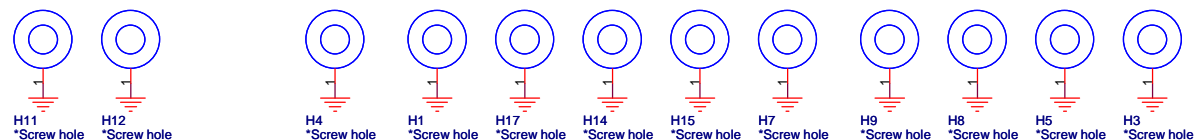
Hole

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CPU Heat Sink



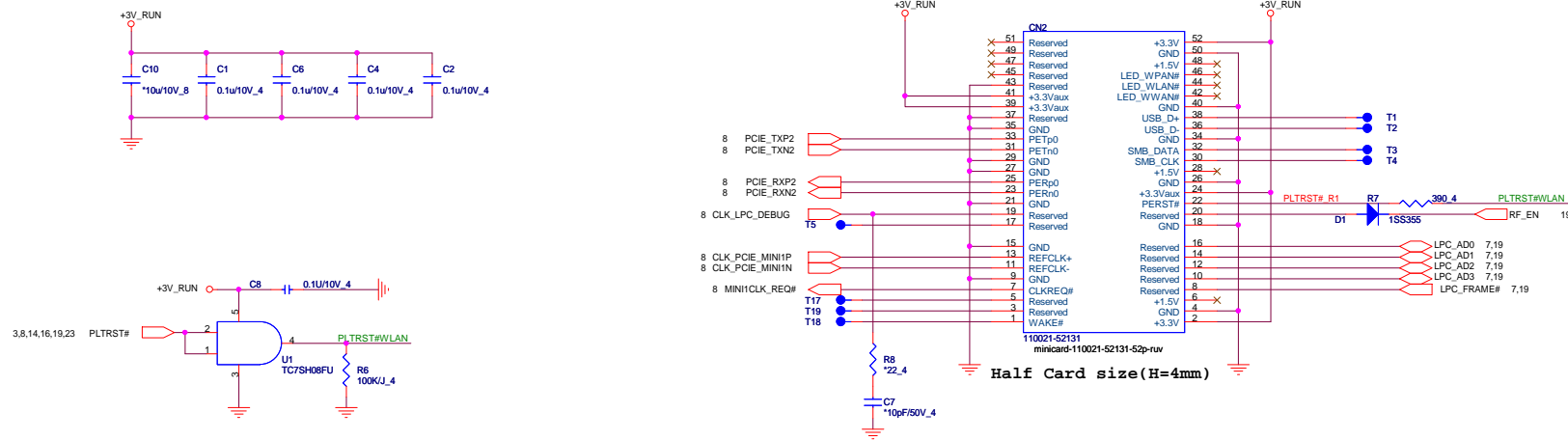
TV module



PCH Heat Sink



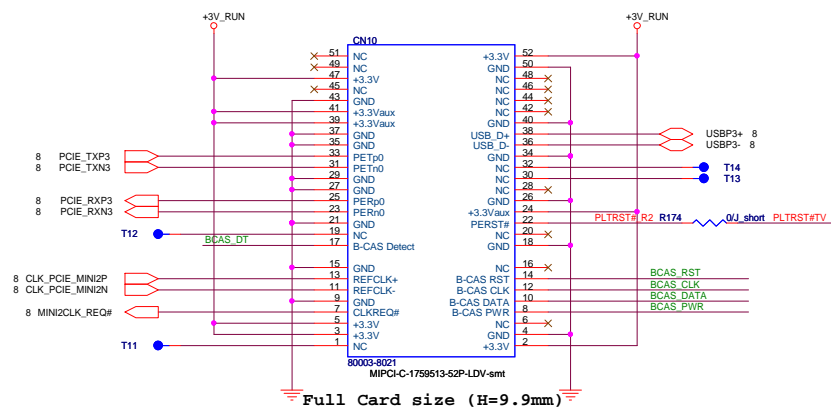
MINI CARD (WLAN)



Half Card size(H=4mm)

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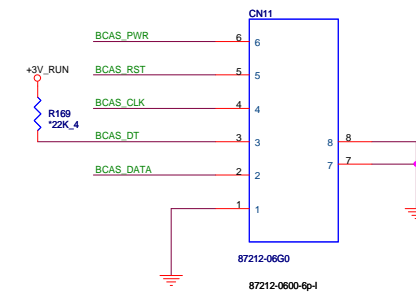
MINI CARD (TV)



Full Card size (H=9.9mm)

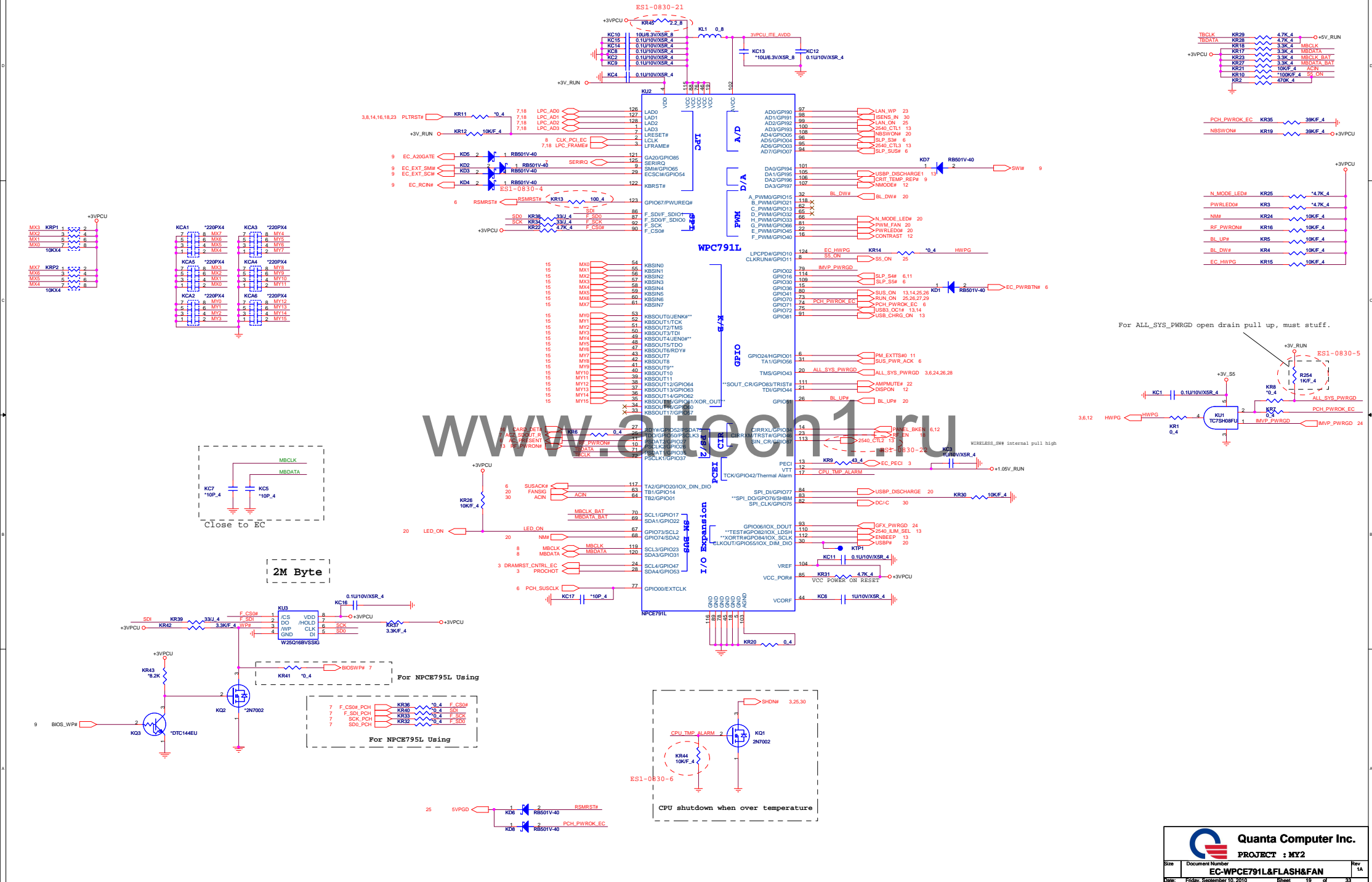
To GT1 BCAS BOARD

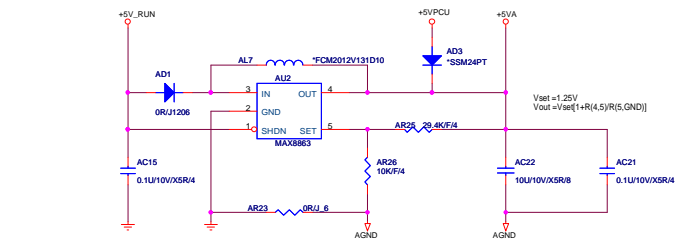
BCAS CONN



KBC-WPCE791L


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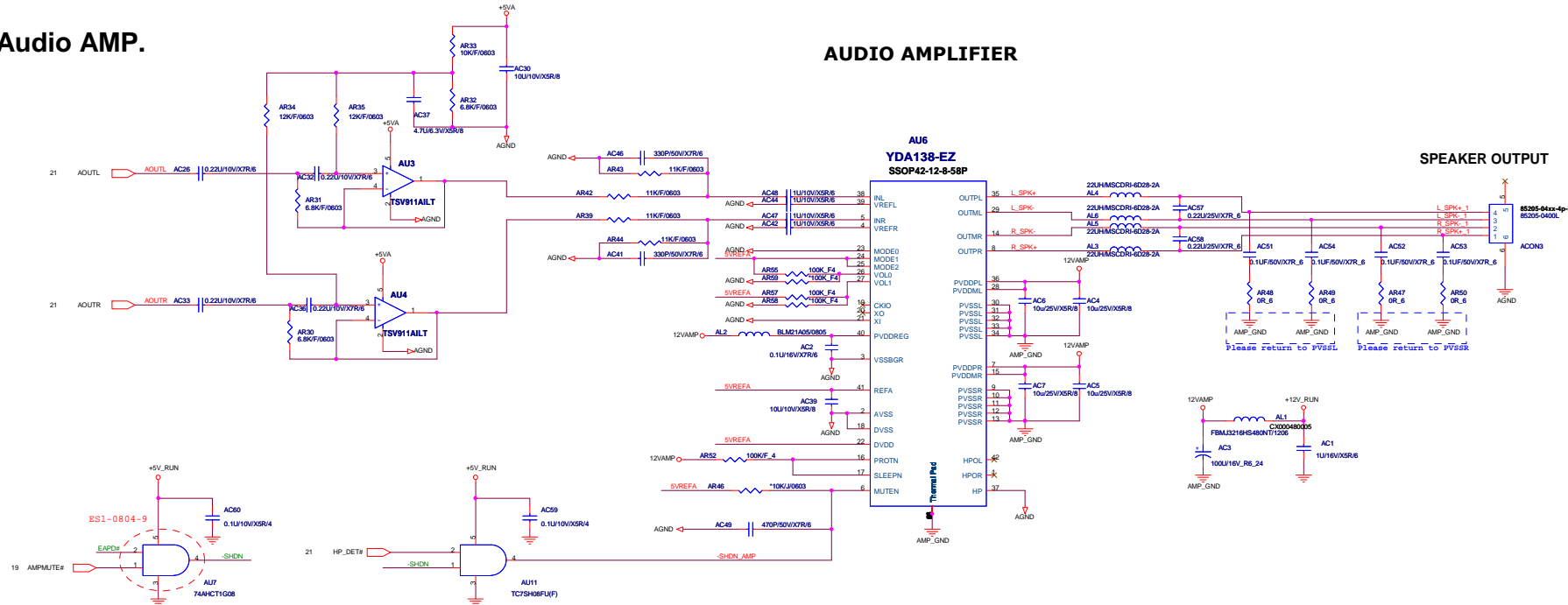


Max. 100mVrms input for Mic-IN

[illegible]

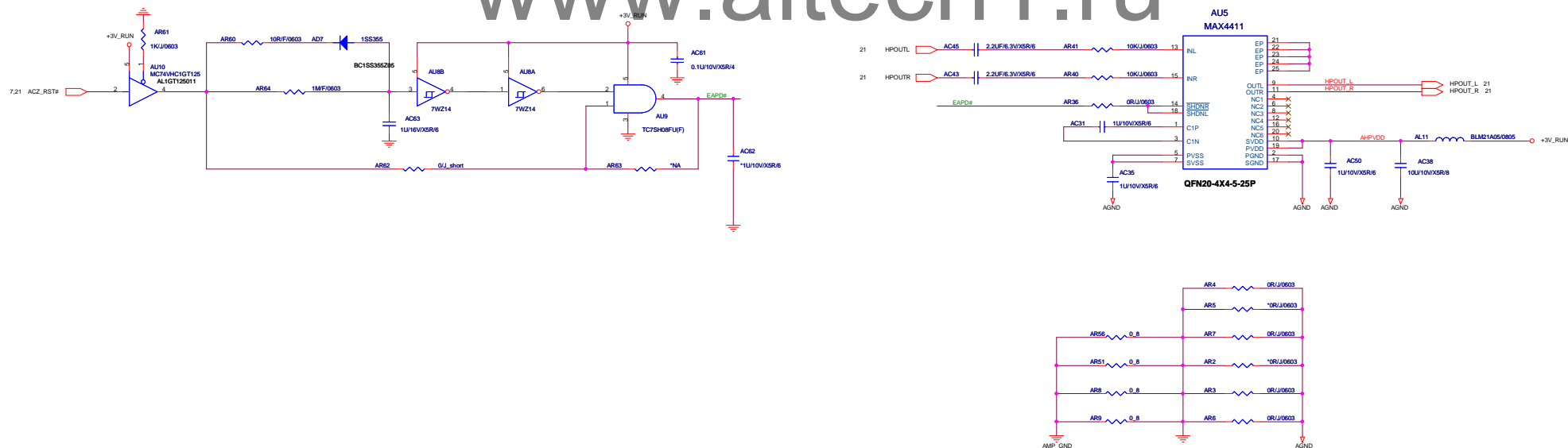
 Quanta Computer Inc. PROJECT : MY2	
Size	Document Number Codex_AL262
Date: Thursday, September 09, 2010	Sheet 21 of 33 Rev 1A

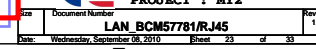
AUDIO AMPLIFIER

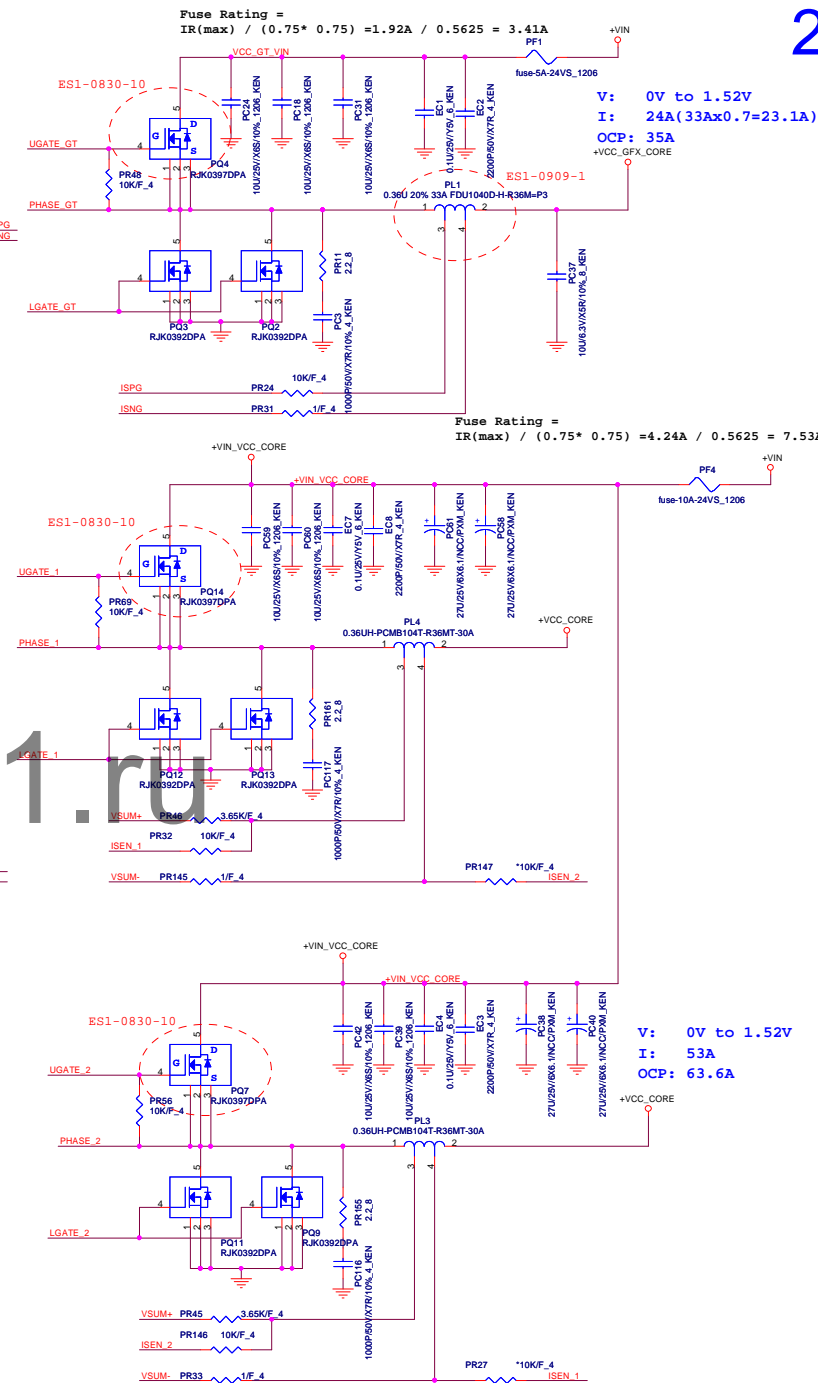


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H.P AMPLIFIER







3.3V & 5V

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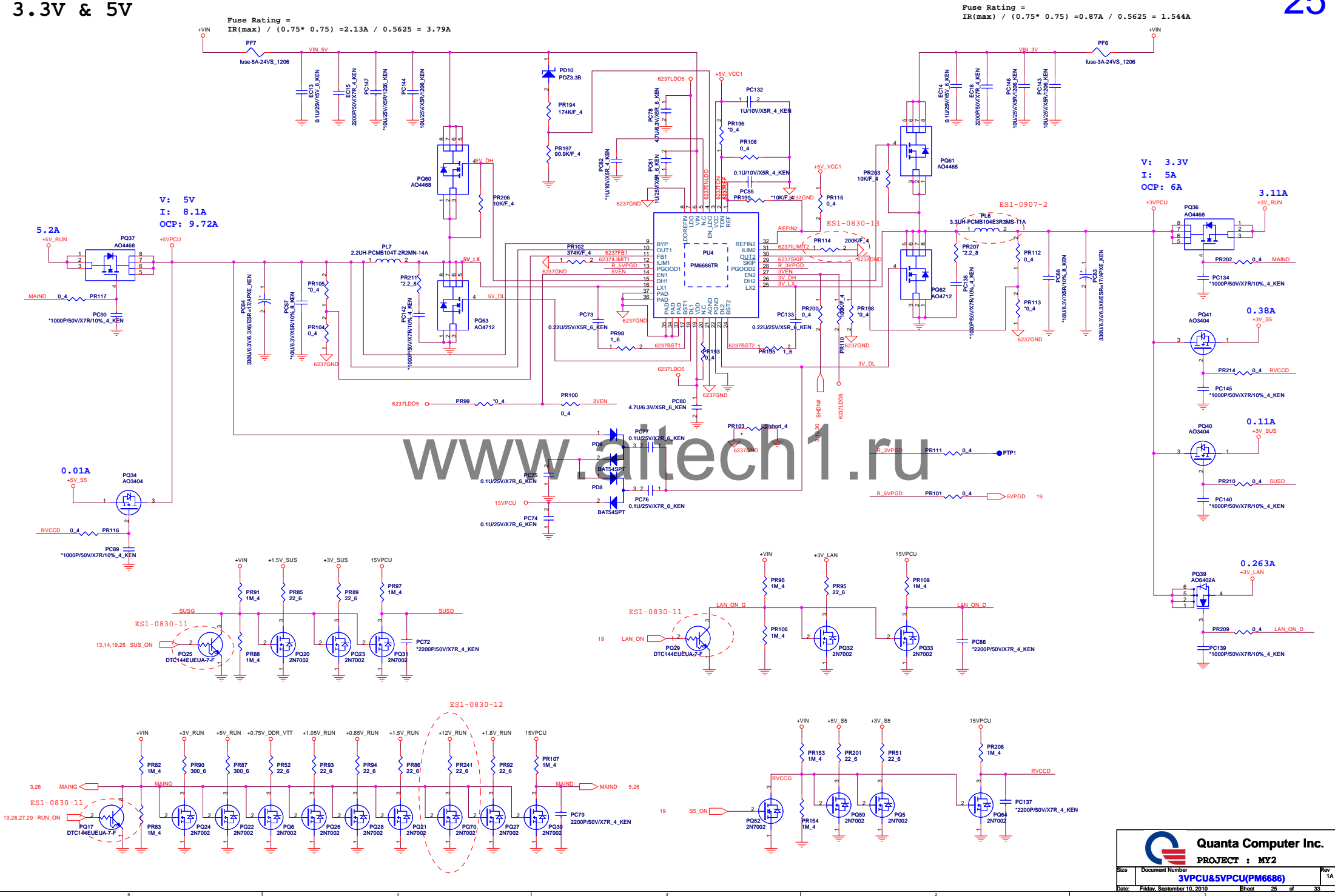
Fuse Rating =
 $IR(max) / (0.75 * 0.75) = 2.13A / 0.5625 = 3.79A$

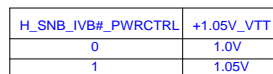
Fuse Rating =
 $IR(max) / (0.75 * 0.75) = 0.87A / 0.5625 = 1.544A$

V: 5V
 I: 8.1A
 OCP: 9.72A

V: 3.3V
 I: 5A
 OCP: 6A

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+0.85V

240 mils

6.0A
+0.85V_RUN

240 mils

VCC1.8

$$V_{out1} = (1 + R_g/R_h) * 0.5$$

60 mils

1.45A
+1.8V_RUN

60 mils

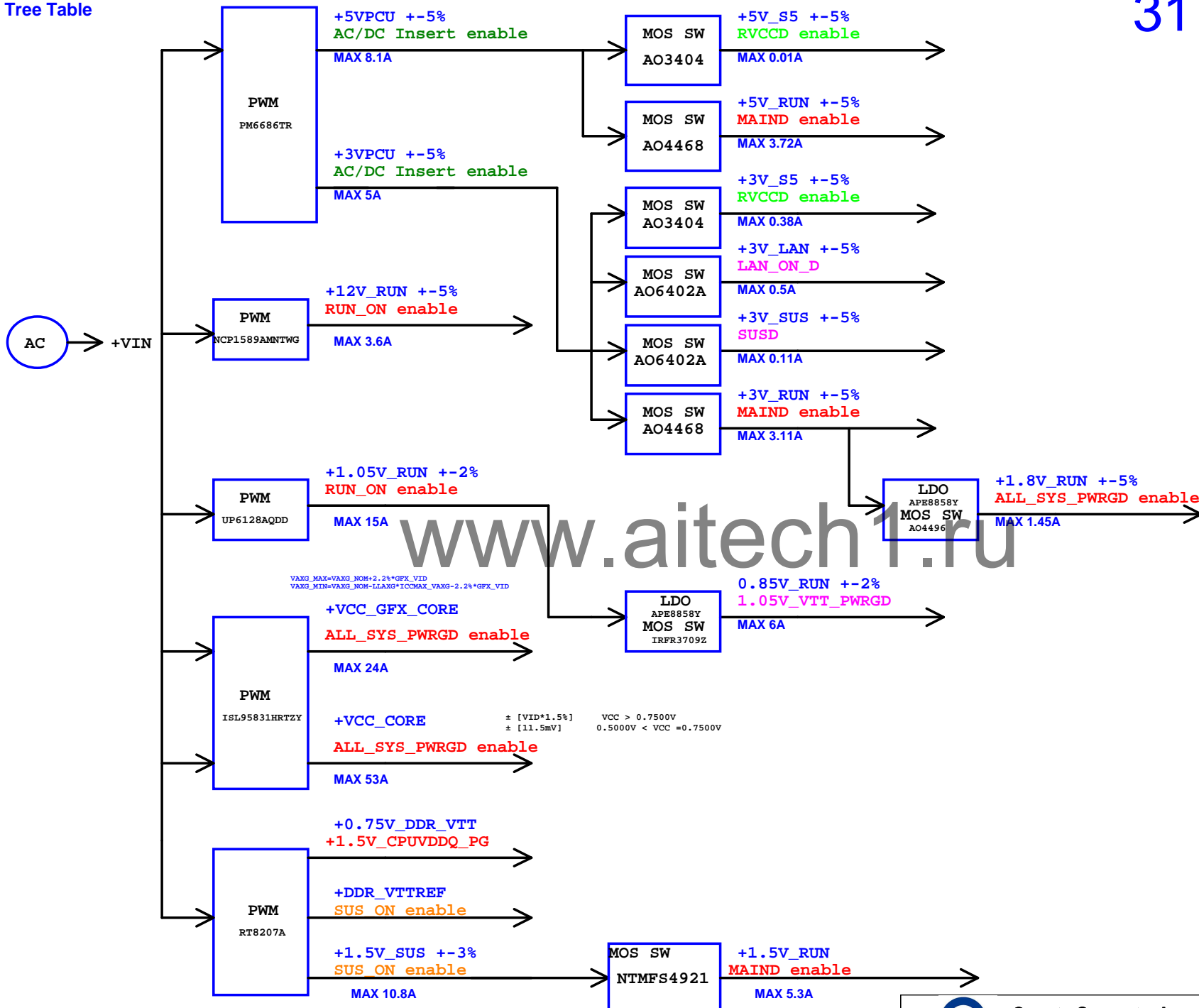
$$V_{out1} = (1 + R_g/R_h) * 0.5$$

VCCSA_SEL	+0.85V
0	0.9V
1	0.8V



Power Tree Table

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Change List

Item	Page	Reason	Detail
2010-08-02	ALL		ES1 release.
ES1-0802-1	3	Change US to open drain type output.	Change US from TC7SH08FU to 74ANCL009.
ES1-0802-2	16	Pin 10 of OZ600BJL1M can't be used as 1.5V_RUN which also used in D0R3.	Remove R23,add R24.
ES1-0802-3	26	change 1.5V_SUS OCP.	Change PR60 from 15K to 7.87K.
ES1-0804-4	24	change for VCC_GFX loadline slop.	Change PR10 from 2.55K to 2.26K.
ES1-0804-5	24	change for VCC_GFX loadline slop.	Change PR28 from 442 to 511.
ES1-0804-6	24	change for VCC_GFX loadline slop.	Change PR38 from 16.5K to 6.65K.
ES1-0804-7	24	change for VCC_GFX loadline slop.	Change PR3 from 18.7K to 15.8K.
ES1-0804-8	24	Correct ROM error.	Change PR119 from 10K to 100K.
ES1-0804-9	22	Correct ROM error.	Change A07 from TC7SH08FU to 74ANCT100B.
ES1-0830-1	7	Solve current leakage on S5.	Change power +3VPCU to +3V_S5.
ES1-0830-2	7	Correct SPI ROM interface to PCM.	Swap PCM_SPI_80 and PCM_SPI_81.
ES1-0830-3	14	Change capacitor of USB 3.0 crystal for frequency precision.	Change C157, C168 from 15P to 12P.
ES1-0830-4	19	Correct voltage level of RSMRST#.	Change KR13 from 2.2K to100.
ES1-0830-5	19	Correct voltage level of ALL_SYS_PWRGD.	Change R254 from 100K to 1K.
ES1-0830-6	19	To avoid glitch when EC are resetting.	Add a pull low resistor KR44 10K.
ES1-0830-7	20	Correct SATA LED abnormal.	Add a pull high resistor R449 10K.
ES1-0830-8	24	Modify VCC_GFX loadline slop.	change PR10 from 2.26K to 2.15K
ES1-0830-9	24	Modify VCC_GFX loadline slop.	Change PR20 from 3.32K to 3.24K.
ES1-0830-10	24,26,27	Change Footprint of MOSFET.	Change PQ4, PQ14, PQ7, PQ10, PQ53, PQ54 form NTMFS4921NT1G to RUX0397DPA
ES1-0830-11	25	Change vendor of transistor.	Change Vendor of PQ25, PQ17, PQ29.
ES1-0830-12	25	Add current discharge of +12V_RUN.	Add PR241, PQ70.
ES1-0830-13	25	Follow OCP of +3VPCU.	change PR114 from 220K to 200K.
ES1-0830-14	26	Meet power sequence of +1.5V_RUN and +0.75V_DDR_VTT.	Change PR77 from 100K to 820K and add PQ71.
ES1-0830-15	27	Follow OCP of +1.05V.	Change PR169 from 3.65K to 3.32K
ES1-0830-16	28	Change footprint.	Change footprint of PQ55.
ES1-0830-17	29	Follow OCP of +12V_RUN.	Change PR226 from 10K to 6.34K.
ES1-0830-18	30	Make VIN work normally during adapter insert.	Add PC168 4.7u.
ES1-0830-19	30	Modify OVP threshold VA+.	Change PD1 from 22V to 26V, PR130 from 1K to 47K, PR131 from 10K to 100K.
ES1-0830-20	26	Follow OCP of +1.5V_SUS.	Change PR60 from 7.87K to 5.23K.
ES1-0830-21	26	Follow suggestion of EC vendor Nuvoton.	Add ER45 2.2 ohm.
ES1-0830-22	13,19	Add more control pin for TPS2540.	Connect 2540_CTL2 to EC.
ES1-0830-23	24	Add buffer of ALL_SYS_PWRGD to VR_ON of CPU and GFX CORE.	Add PU12, PR243 but reserved.
ES1-0830-24	24	Follow intel SPEC danamic VID slew rate.	Add PR242, PC169, PR13, PC170.
ES1-0830-25	27	Manufacture change P/N.	Manufacture change P/N of PU7.
ES1-0901-1	14	Change vendor.(Refer to ES1-0907-1.)	Change vendor from ALLTOP to SUYIN.
ES1-0901-2	14	Change ESD component as NEC approved.	Change component to IP4284CE10-TB but reserved.
ES1-0901-3	16	For EMI card reader clock issue.	Add 5P capacitor at C413.
ES1-0901-4	16	Follow vendor's suggestion, change value of C290.	Change C290 from 0.01u to 4.7u.
ES1-0903-1	30	For DC-in reverse voltage protect.	Change PD13 to serial connection with PD15.
ES1-0903-2	17	Follow thermal team's suggestion, change CPU thermal bracket.	Change CPU thermal bracket.
ES1-0906-1	3	For consistency of power state, change power source of U8 pin5.	Change from +3V_RUN to +3V_SUS.
ES1-0906-2	3	For future's CPU feature, connect VCCIO_SEL.	Add R289.
ES1-0906-3	7	Follow FF3, add pull high/low resistor for PCM_JTAG_TDO_R.	Add R450, R451.
ES1-0907-1	14	Follow NECP's request, change vendor back to ALLTOP.	Change vendor of CON3 from SUYIN back to ALLTOP.
ES1-0907-2	27	change 3VPCU OCP target	change PL6 from 3.8uH to 3.3uH
ES1-0908-1	7	Add damping resistor for LPC waveform glitch and ringing.	Add R452, R453, R454, R455.
ES1-0908-2	7	Change OSD SATA port.	Change SATA port from port2 to port0.
ES1-0908-3	21	Add capacitor for audio ACK_SDIO# glitch and ringing.	Add AC10.
ES1-0909-1	24	GFX load from 24 to 33	PL1 change from DC+36V0M000 to DC+36V0M000

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